Amendments to the Claims:

1. (previously presented) A system to initiate, by a host, an event in a first device, the system comprising:

a signal line to communicate a plurality of data values between a host and one or more second devices; and

a tap line to communicate said plurality of data values between said signal line and said first device;

wherein said event is initiated upon detection, by said first device, of a predetermined sequence of address locations on the tap line,

and wherein said event selectively switches a communication path from a third device to one of said host and said first device.

2. (previously presented) The system of claim 1, wherein the event comprises a switching from a communication path between the first device and the third device and a communication path between the signal line and the third device.

3. (previously presented) The system of claim 1, wherein the event comprises a switching from a communication path between a signal line and the third device and a communication path between the first device and the third device.

4. (original) The system of claim 1, wherein the host is a processor.

5. (original) The system of claim 1, wherein the first device is a logic device.

6. (original) The system of claim 1, wherein each of the one or more second devices is a memory device.

7. (original) The system of claim 1, wherein the third device is a memory device.

8. (original) The system of claim 1, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

9. (previously presented) The system of claim 1, wherein each of the plurality of data values represents a memory location within any of the one or more second devices.

10. (original) The system of claim 9, wherein utilization of a data value provides a call to the represented memory location.

11. (previously presented) A method to initiate, by a host, an event in a first device comprising:

communicating, by a signal line, a plurality of data values between a host and one or more second devices;

communicating, by a tap line, said plurality of data values between said signal line and said first device;

initiating said event upon detection by said first device of a predetermined sequence of address locations on the tap line; and

selectively switching a communication path from a third device to one of the host and the first device, in response to said detection.

12. (previously presented) The method of claim 11, wherein the event comprises a switching from a communication path between the first device and the third device and a communication path between the signal line and the third device.

13. (previously presented) The method of claim 11, wherein the event comprises a switching from a communication path between a signal line and the third device and a communication path between the first device and the third device.

14. (original) The method of claim 11, wherein the host is a processor.

15. (original) The method of claim 11, wherein the first device is a logic device.

16. (original) The method of claim 11, wherein each of the one or more second devices is a memory device.

17. (original) The method of claim 11, wherein the third device is a memory device.

18. (original) The method of claim 11, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

19. (previously presented) The method of claim 11, wherein each of the plurality of data values represents a memory location within any of the one or more second devices.

20. (original) The method of claim 19, wherein utilization of a data value provides a call to the represented memory location.

21. (previously presented) A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to initiate, by a host, an event in a first device comprising:

communicating, by a signal line, a plurality of data values between a host and one or more second devices;

communicating, by a tap line, said plurality of data values between said signal line and said first device;

initiating said event upon detection by said first device of a predetermined sequence of address locations on the tap line; and

selectively switching a communication path from a third device to one of the host and the first device, in response to said detection.

22. (previously presented) The set of instructions of claim 21, wherein the event comprises a switching from a communication path between the first device and the third device and a communication path between the signal line and the third device.

23. (previously presented) The set of instructions of claim 21, wherein the event comprises a switching from a communication path between a signal line and the third device and a communication path between the first device and the third device.

24. (original) The set of instructions of claim 21, wherein the host is a processor.

25. (original) The set of instructions of claim 21, wherein the first device is a logic device.

26. (original) The set of instructions of claim 21, wherein each of the one or more second devices is a memory device.

27. (original) The set of instructions of claim 21, wherein the third device is a memory device.

28. (original) The set of instructions of claim 21, wherein the host is a microprocessor chipset, the first device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access Memory (SDRAM).

29. (previously presented) The set of instructions of claim 21, wherein each of the plurality of data values represents a memory location within any of the one or more second devices.

30. (original) The set of instructions of claim 29, wherein utilization of a data value provides a call to the represented memory location.

31. (currently amended) A system comprising:

a first device to execute a variety of computationally intensive tasks;

a memory bus directly coupled to both a host and one or more second devices, the memory bus to communicate a plurality of data values between the host and said one or more second devices;

a tap line to communicate said plurality of data values between the memory bus and the first device; and

a memory device selectively coupled, by a bus switch line ~~and the memory bus~~, to one of the host and first device, wherein the bus switch line is coupled with the memory device and the bus switch line is selectively switched between the first device and the host in response to an event initiation.

32. (previously presented) The system as recited in claim 31,wherein the tap line communicatively connects the first device with the host via the memory bus, and wherein a sequence of control signals sent from the host to the first device cause an event initiation.

33. (previously presented) The system as recited in claim 32, wherein the sequence of control signals comprise a sequence of address locations.

34. (previously presented) The system as recited in claim 33, wherein the one or more second devices comprise memory devices, and wherein the address locations represent memory locations within any of the one or more second devices.

35. (previously presented) The system as recited in claim 31, wherein the first device is a field programmable gate array (FPGA).

36. (previously presented) The system as recited in claim 35, wherein the memory device is a synchronous dynamic random access memory (SDRAM).

37. (previously presented) The system as recited in claim 36, wherein the one or more second devices comprise one or more dual in-line memory modules (DIMMs).

38. (previously presented) The system as recited in claim 31, wherein an event initiation is to be controlled by the host and the selective switching of the bus switch is to be controlled by the first device.

39. (currently amended) A system comprising:

a first device to execute a variety of computationally intensive tasks;

a memory bus to communicate a plurality of data values between a host and one or more second devices;

a tap line to communicate said plurality of data values between the memory bus and the first device, wherein the tap line communicatively connects the first device with the host via the memory bus, and wherein a sequence of control signals comprising a sequence of address locations is sent from the host to the first device to cause an event initiation; and

a memory device selectively coupled, by a bus switch line ~~and the memory bus~~, to one of the host and first device, wherein the bus switch line is coupled with the memory device and the bus switch line is selectively switched between the first device and the host in response to an event initiation.

40. (previously presented) The system as recited in claim 39, wherein the one or more second devices comprise memory devices, and wherein the address locations represent memory locations within any of the one or more second devices.